

FIG. 1A

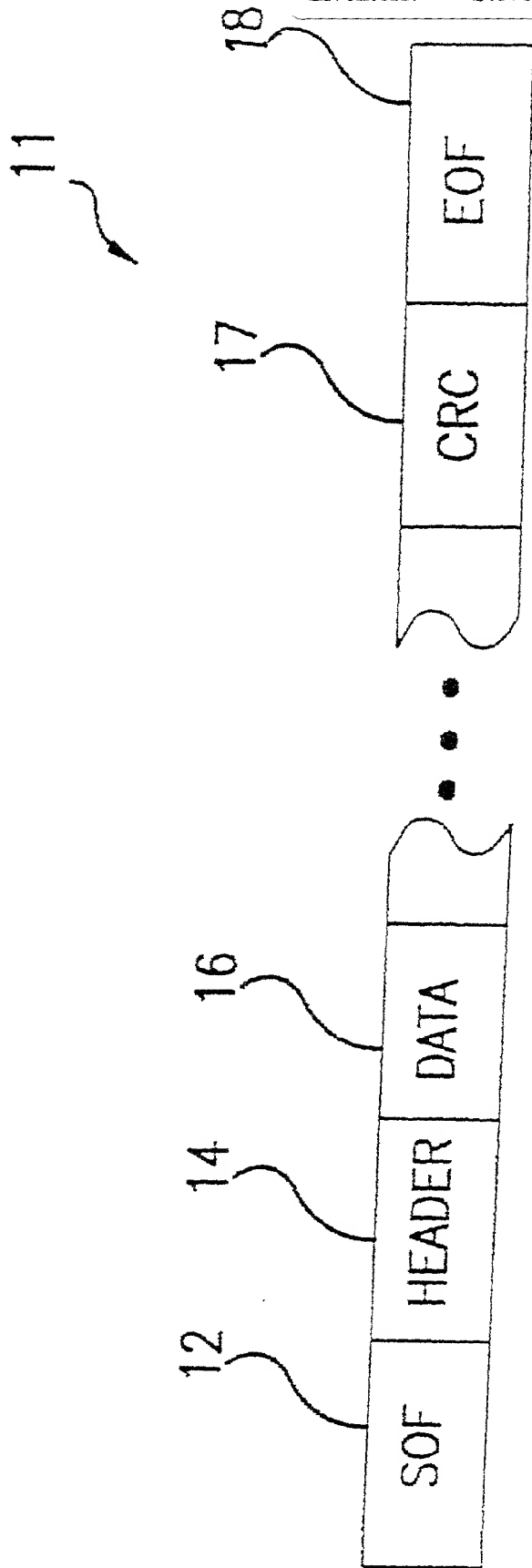


FIG. 1A
PRIOR ART

FIG. 1B

14

Routing Control (R_CTRL)	Destination ID (D_ID)
Class Specific Control (CS_CTL)	Source ID (S_ID)
Data Structure Type (TYPE)	Frame Control (F_CTL)
Sequence ID (SEQ_ID)	Data Field Control (DF_CTL)
Originator ID (OX_ID)	Sequence Count (SEQ_CNT)
	Responder ID (RX_ID)
Parameter or Relative Offset	

FIG. 1B
PRIOR ART

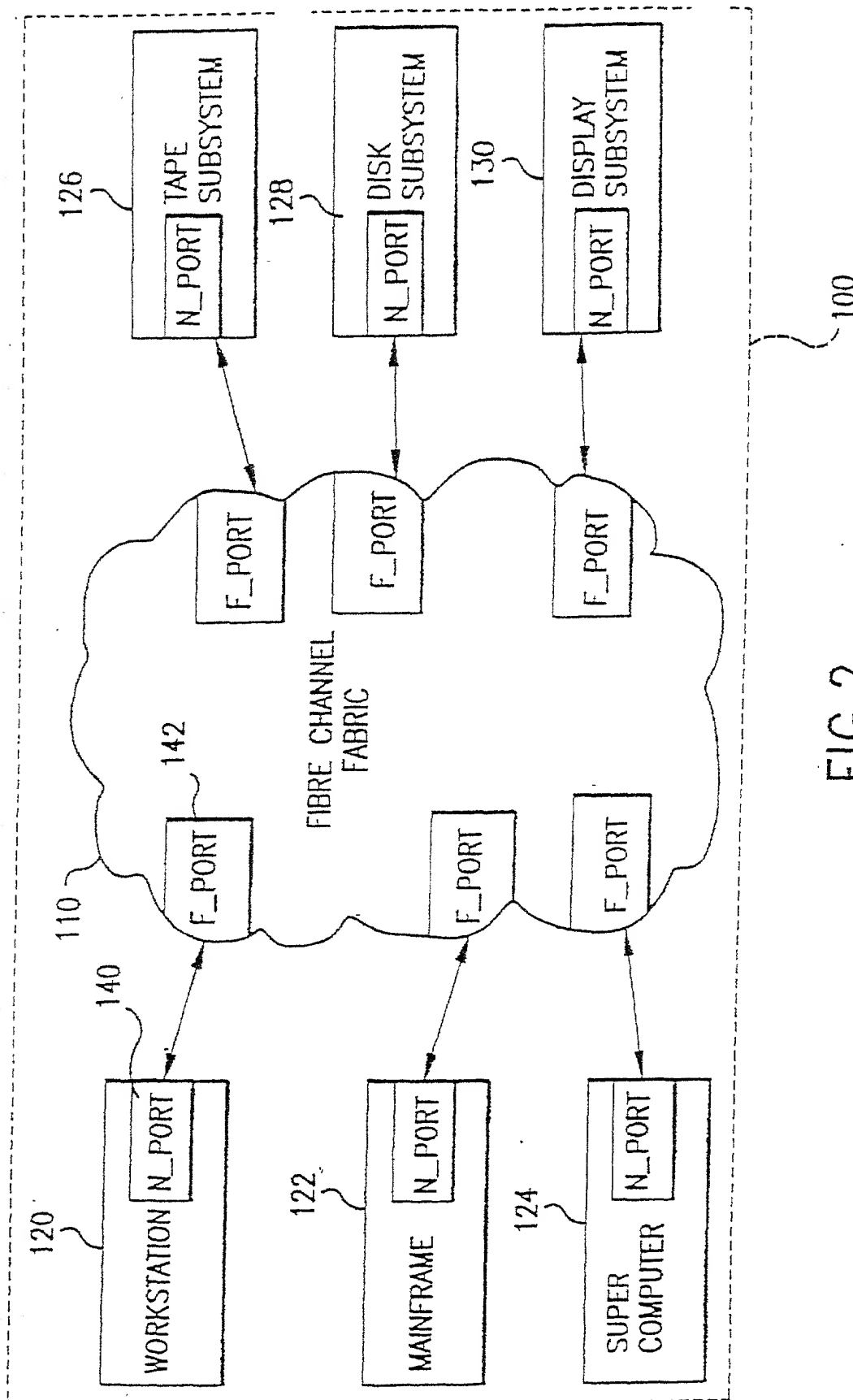


FIG. 2
PRIOR ART

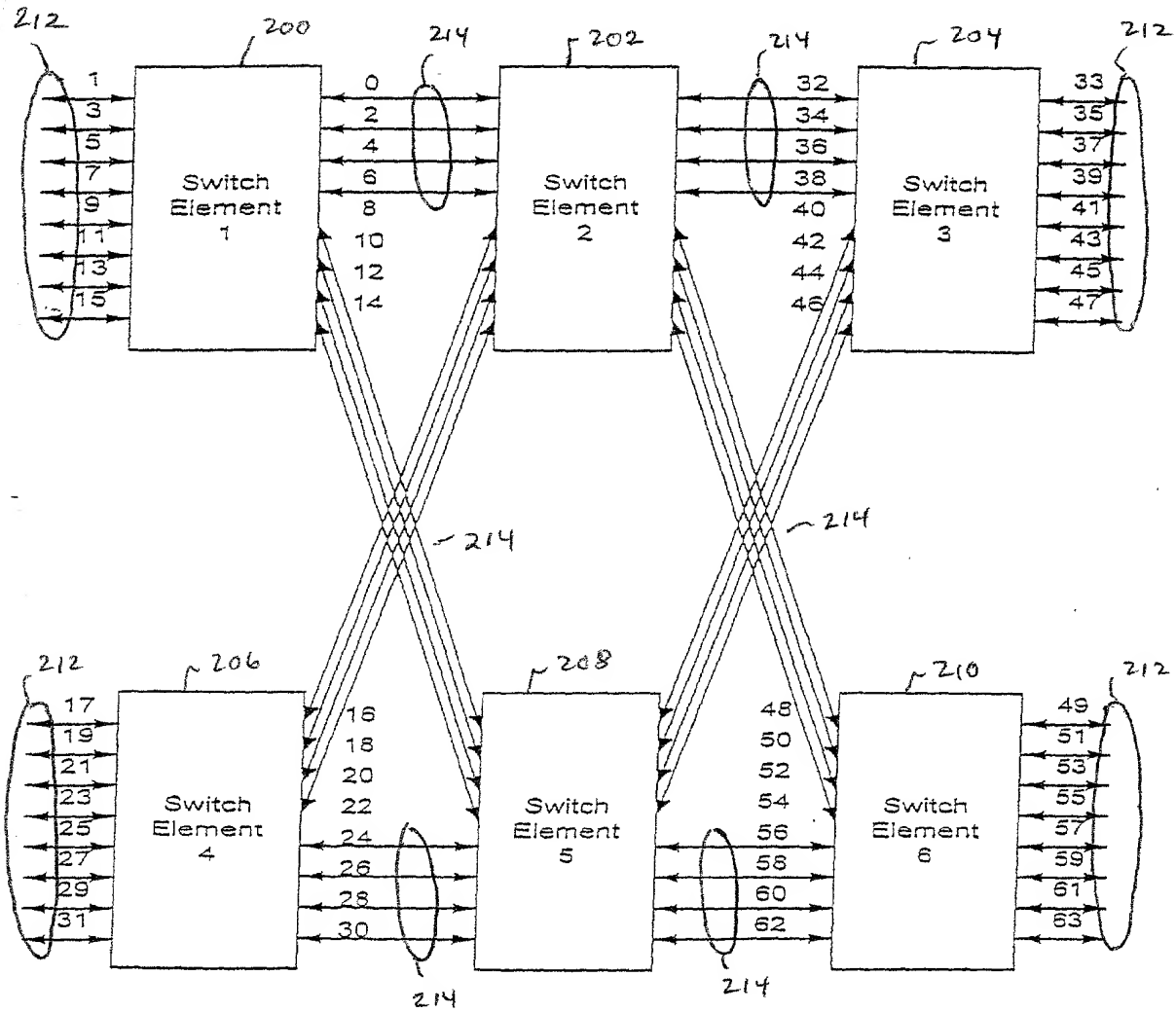


FIG. 3

FOI090" E982/860

Docket/App No.: 2997.1005-001

Title: Fibre Channel Address Adaptor Having Data Buffer Extension...

Inventors: Steven G. Schmidt *et al.*

300 ↘

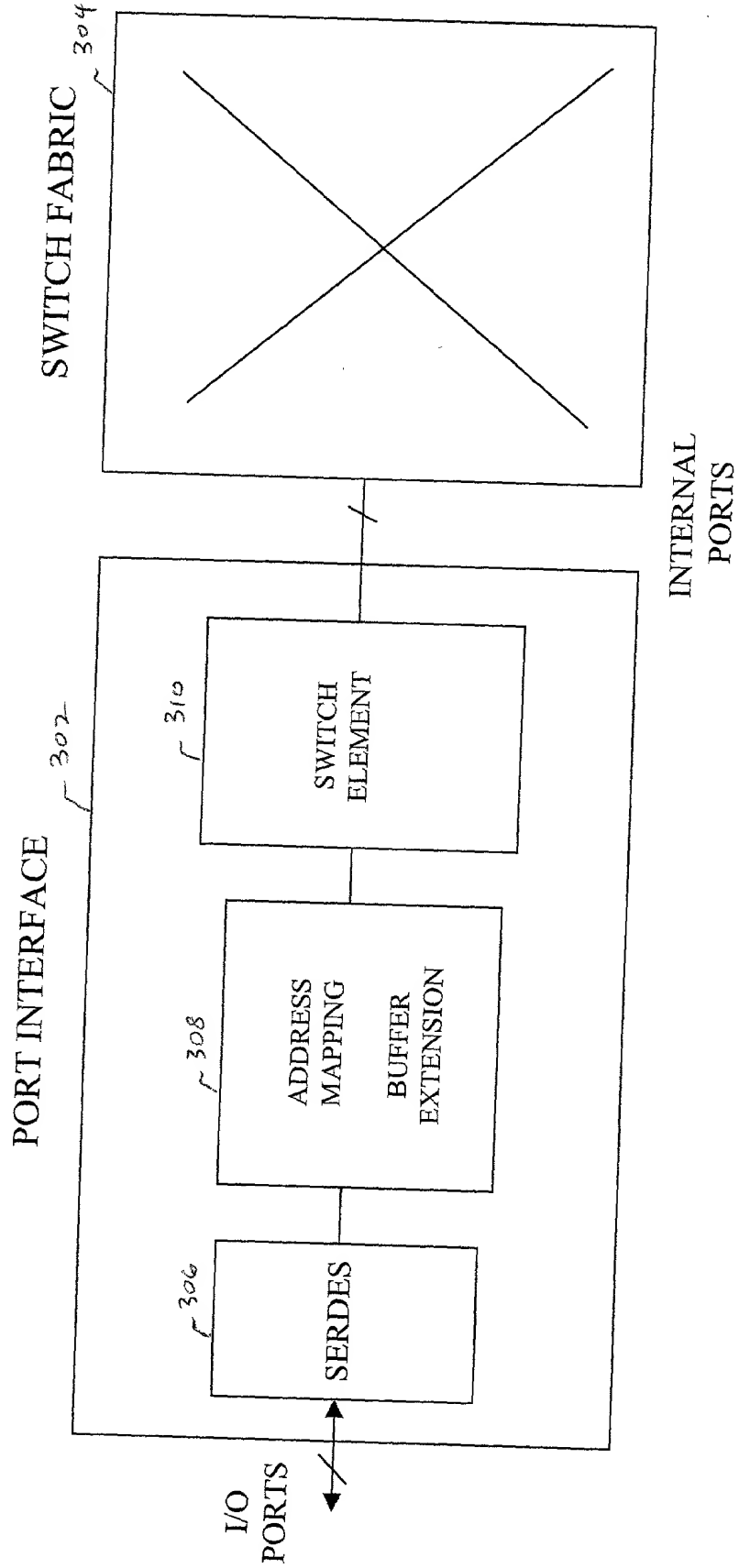


FIG. 4

FOI b7D b7C b7E b7F b7G b7H b7I b7J b7K b7L b7M b7N b7O b7P b7Q b7R b7S b7T b7U b7V b7W b7X b7Y b7Z

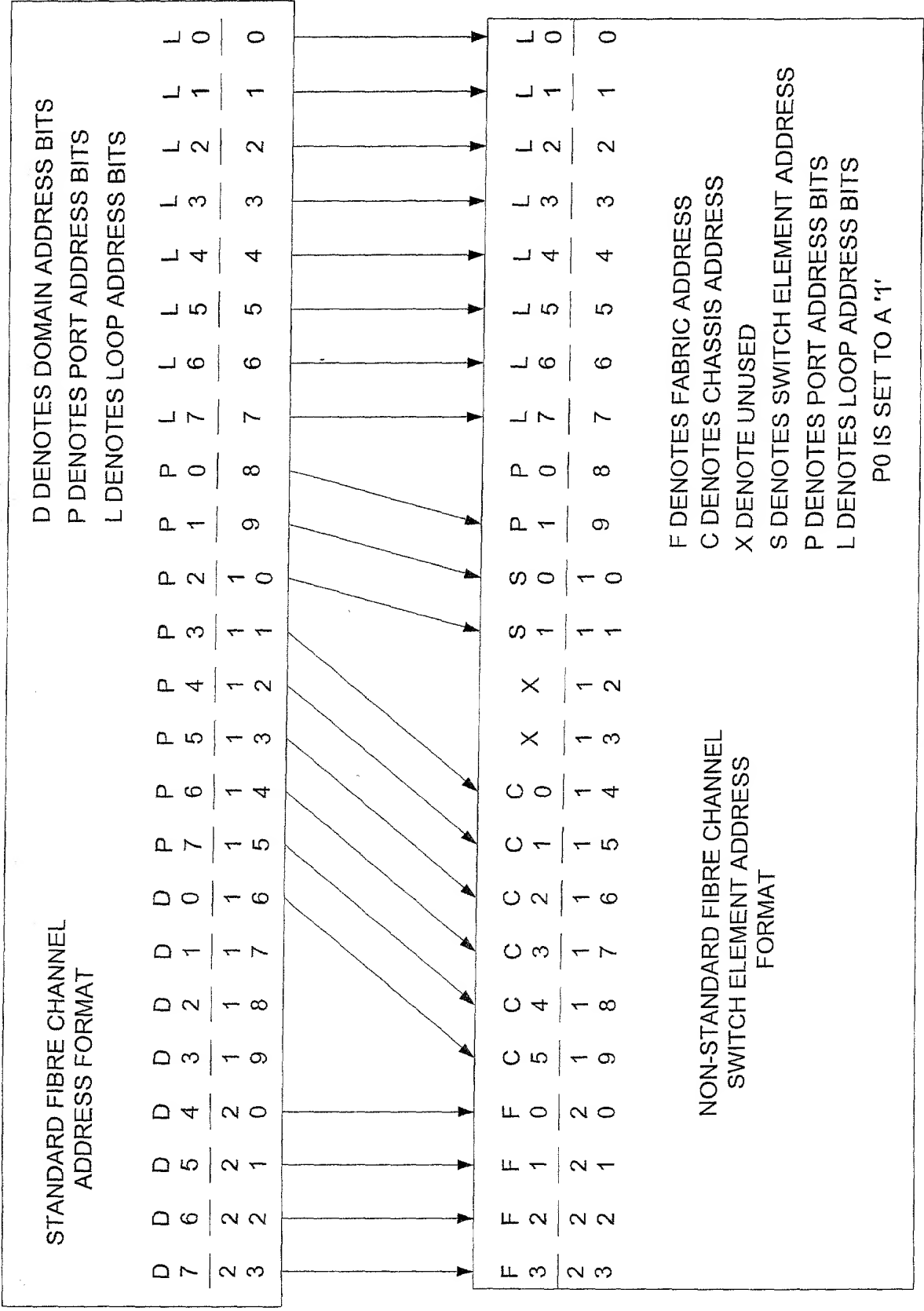


Fig. 5A

FIG. 5B

F DENOTES FABRIC ADDRESS
 C DENOTES CHASSIS ADDRESS
 X DENOTE UNUSED

S DENOTES SWITCH ELEMENT ADDRESS
 P DENOTES PORT ADDRESS BITS
 L DENOTES LOOP ADDRESS BITS

NON-STANDARD FIBRE CHANNEL
 SWITCH ELEMENT ADDRESS
 FORMAT

F	F	F	F	C	C	C	C	C	C	C	X	X	S	S	P	P	L	L	L	L	L	L	L	L	L	L	L	L
3	2	1	0	5	4	3	2	1	0	0	0	0	1	0	1	0	7	6	5	4	3	2	1	0	0	0	0	0
2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0	0	0	0	0
3	2	2	1	0	9	8	7	6	5	4	3	2	1	0														

DOMAIN ADDRESS REGISTER

D	D	D	D	D	D	D	D	D	D	D	P	P	P	P	P	P	P	L	L	L	L	L	L	L	L	L	L	L
7	6	5	4	3	2	1	0	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	0	0	0
2	2	2	2	1	1	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2	1	0	0	0	0
3	2	2	1	0	9	8	7	6	5	4	3	2	1	0														

D DENOTES DOMAIN ADDRESS BITS
 P DENOTES PORT ADDRESS BITS
 L DENOTES LOOP ADDRESS BITS

STANDARD FIBRE CHANNEL
 ADDRESS FORMAT

FIG. 5B

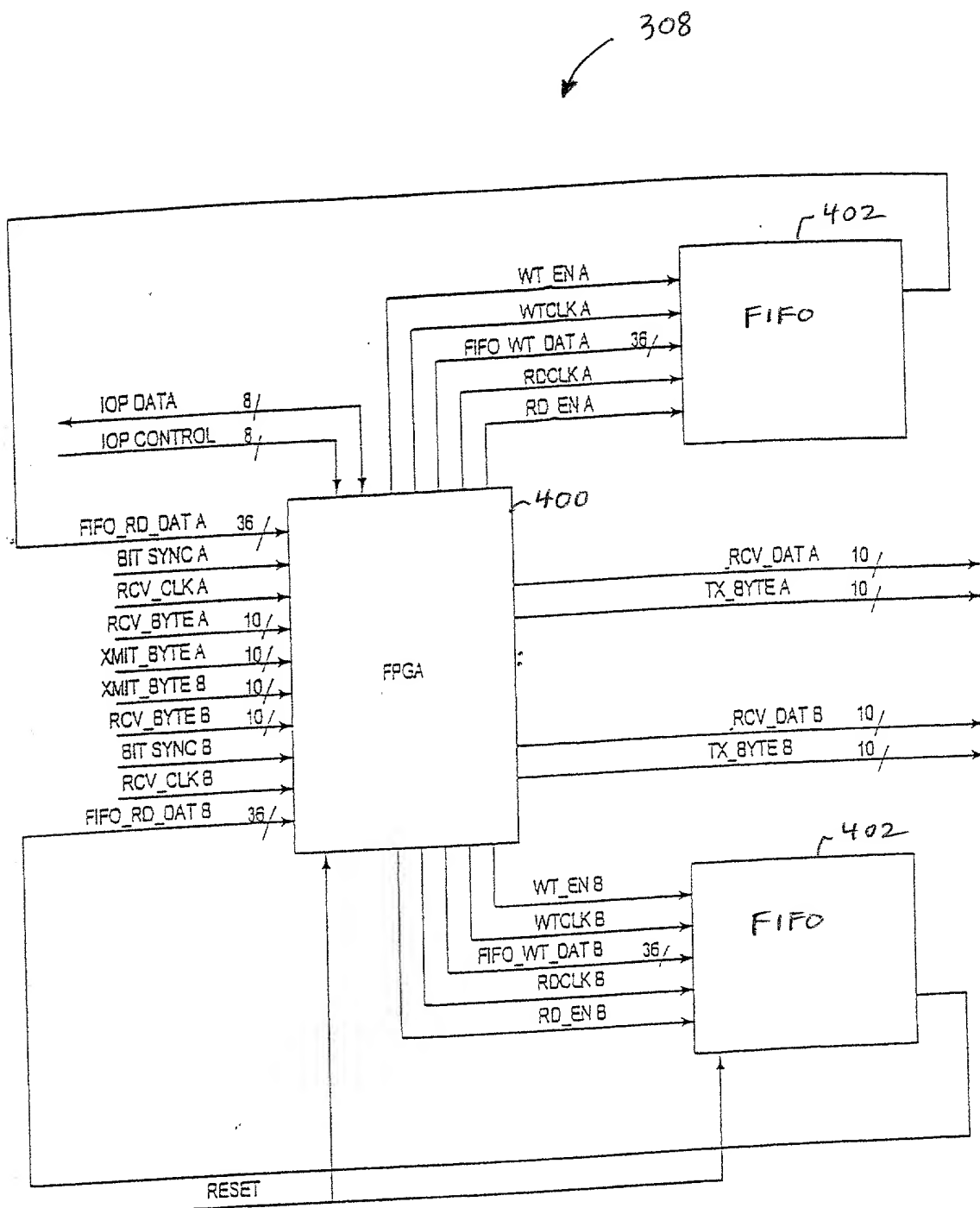


FIG. 6

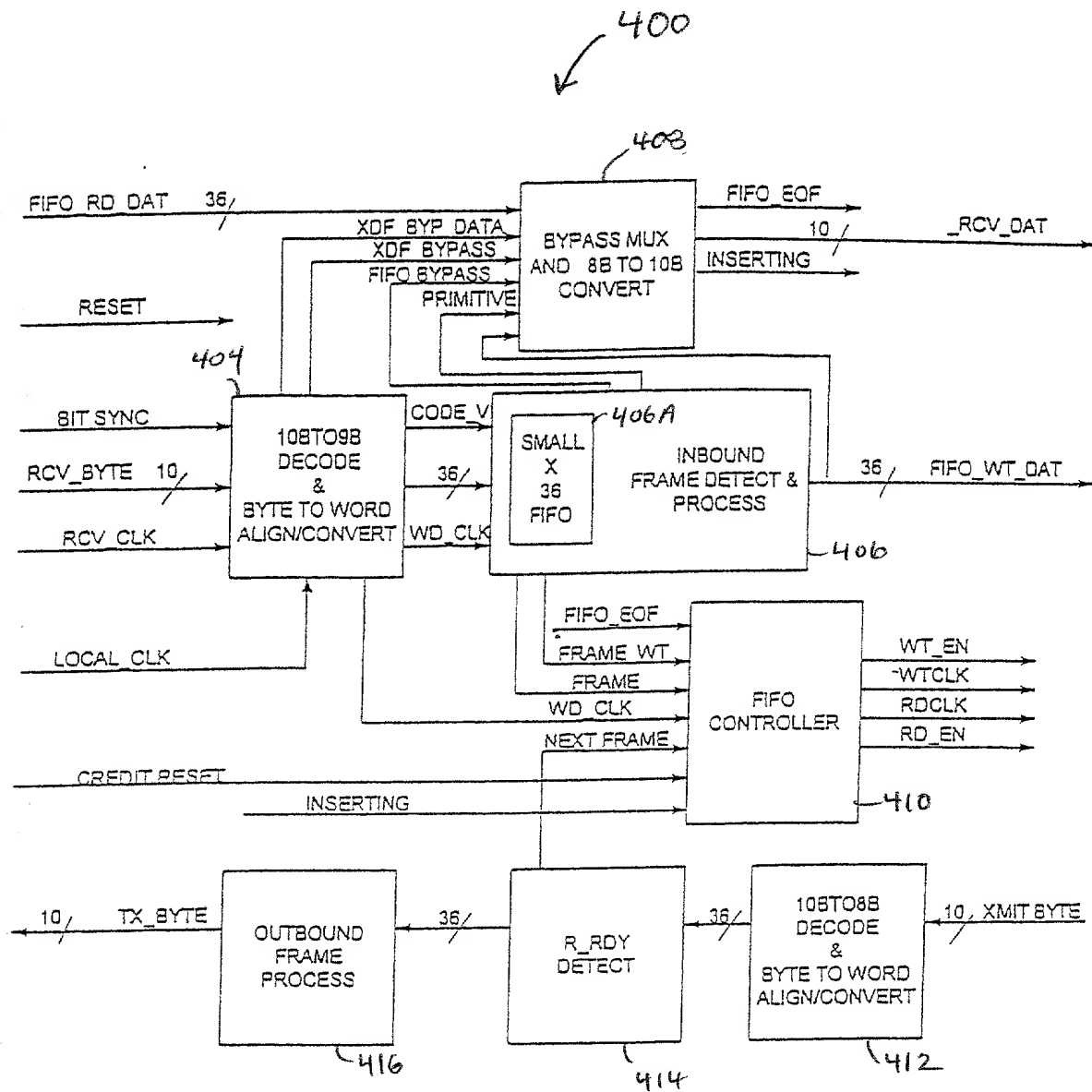


FIG. 7

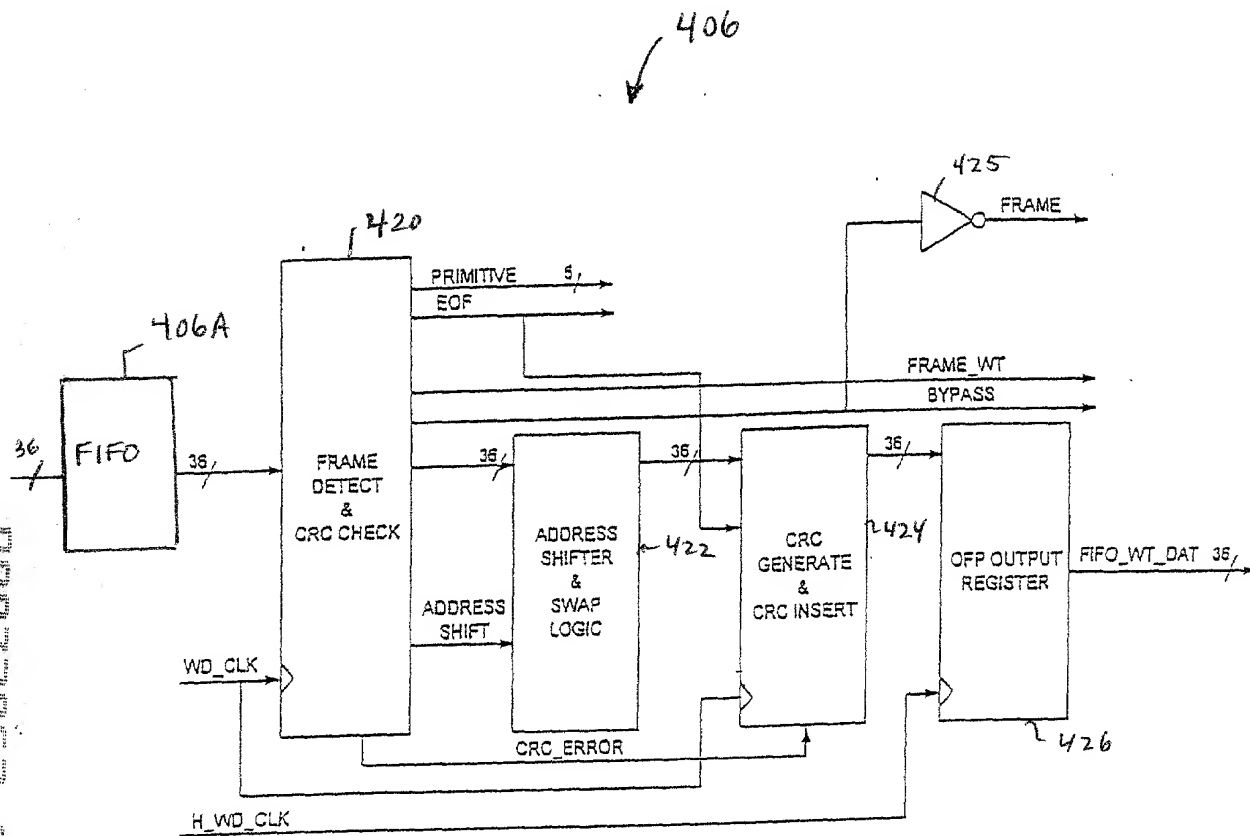


FIG. 8

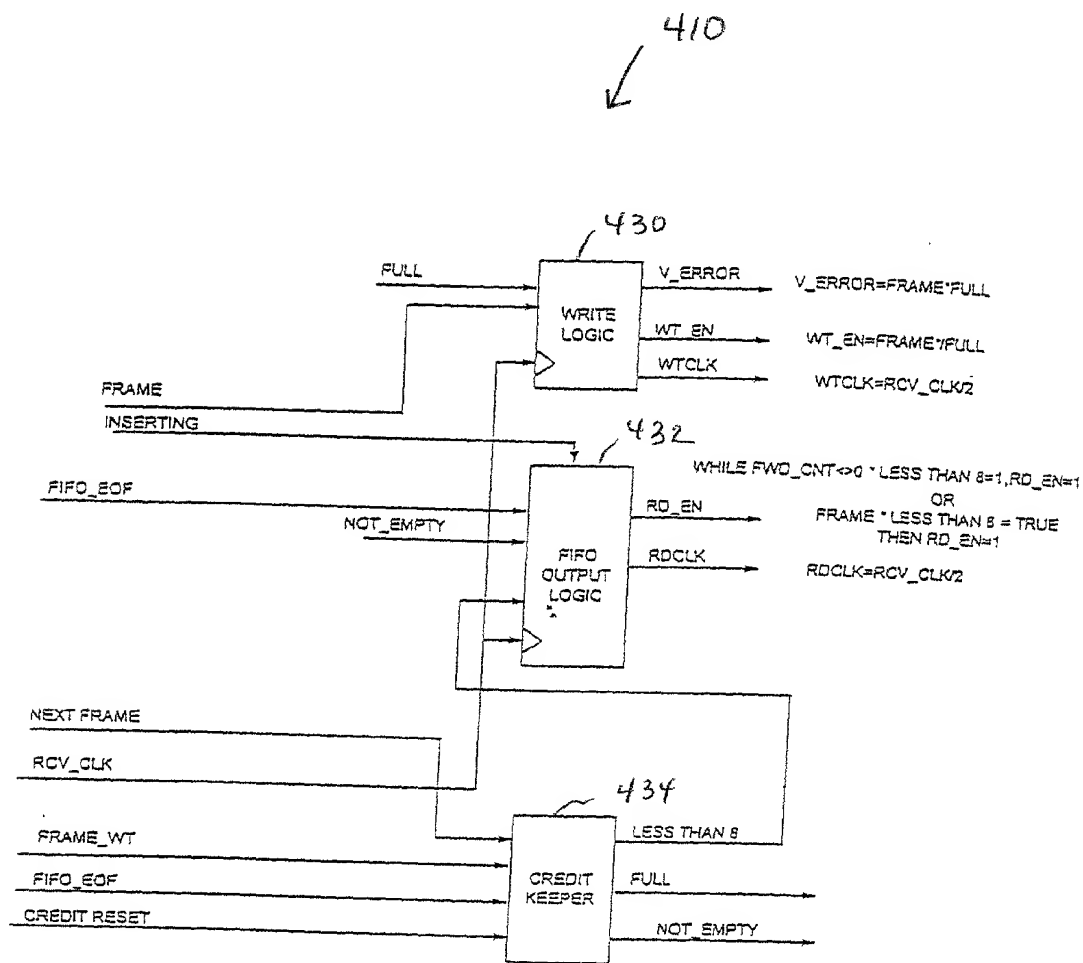


FIG. 9

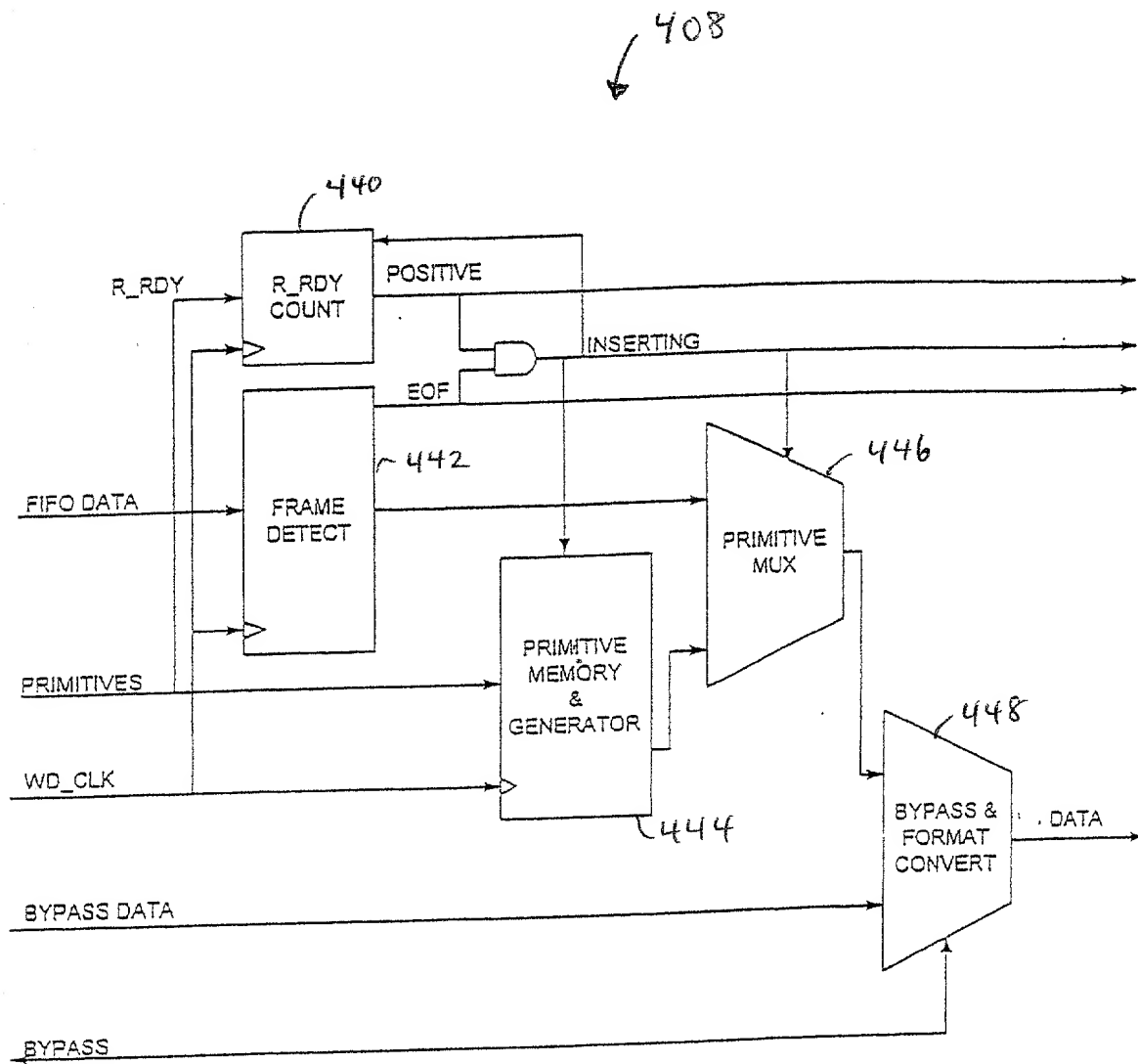


FIG. 10

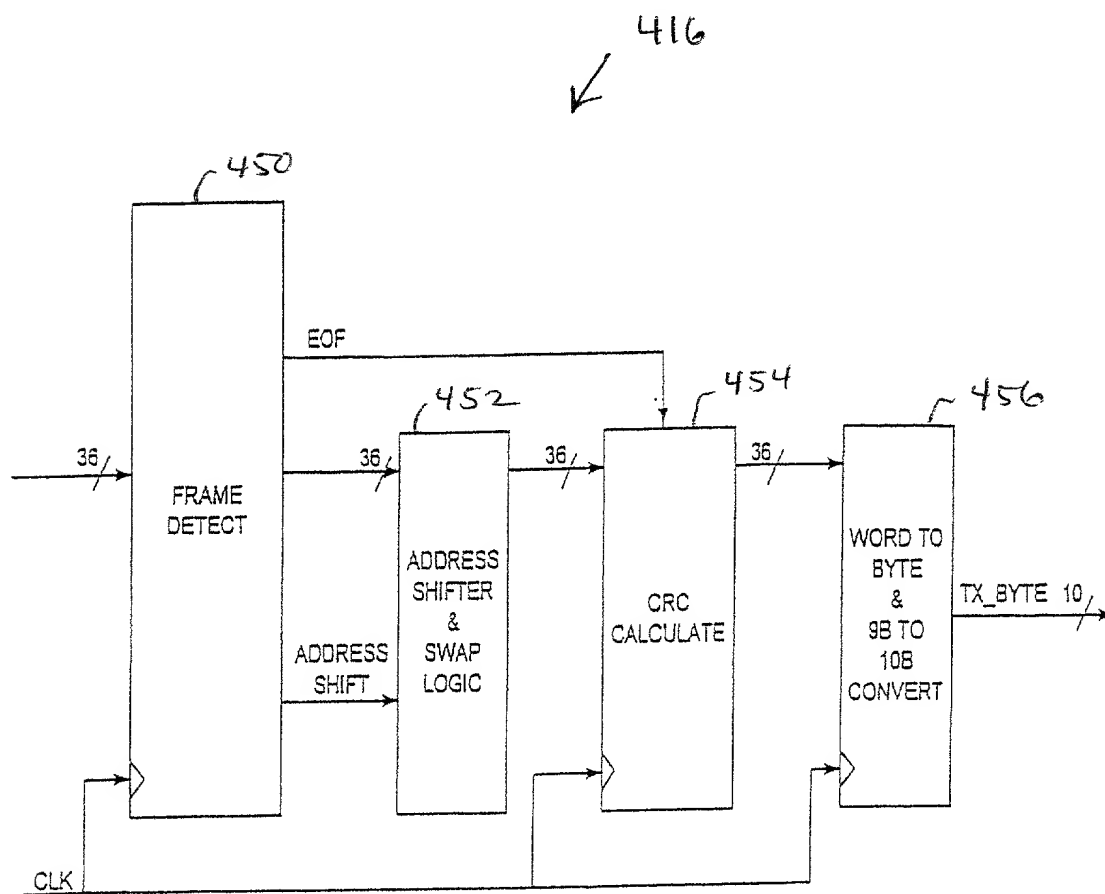


FIG. 11

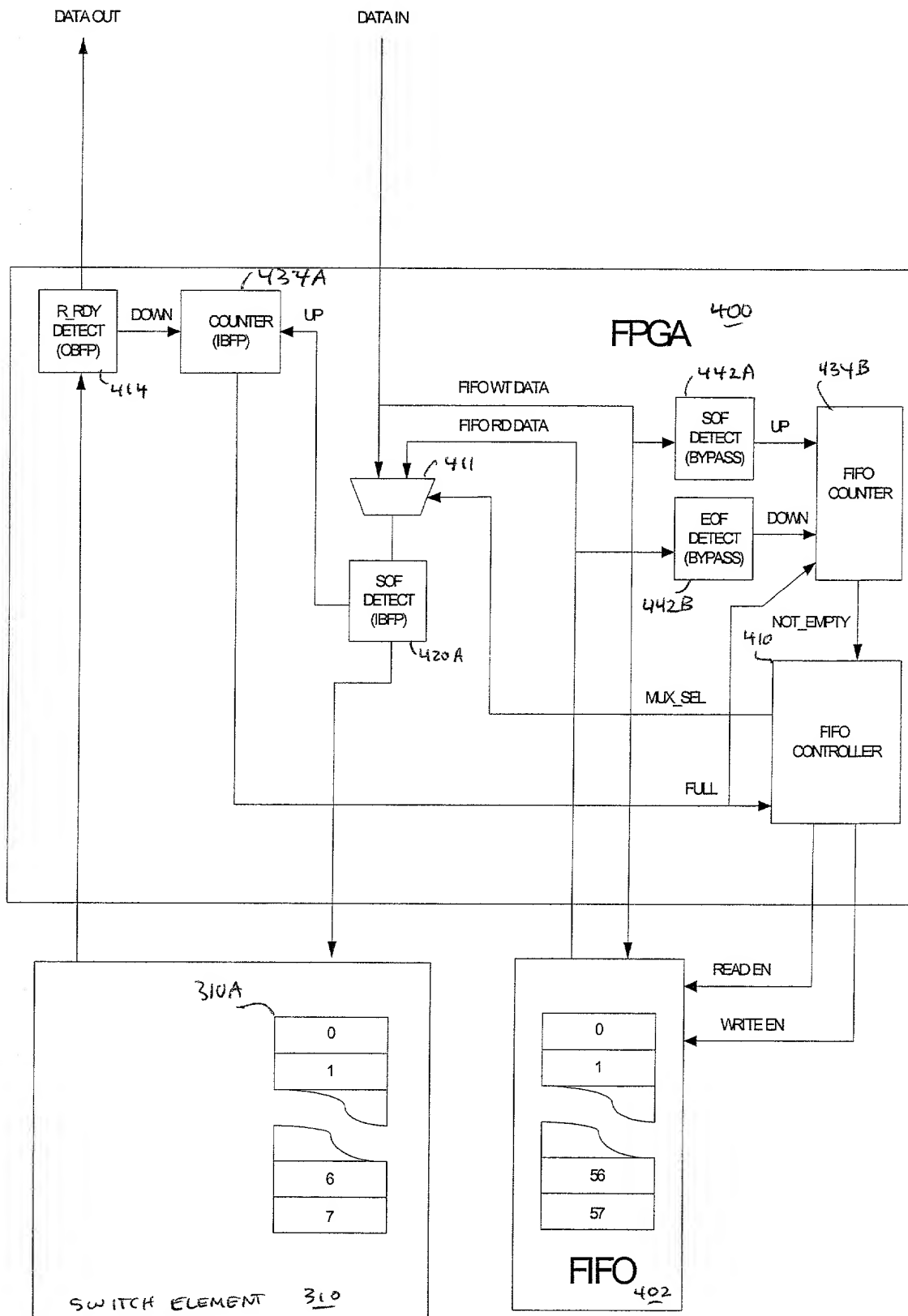


FIG. 12

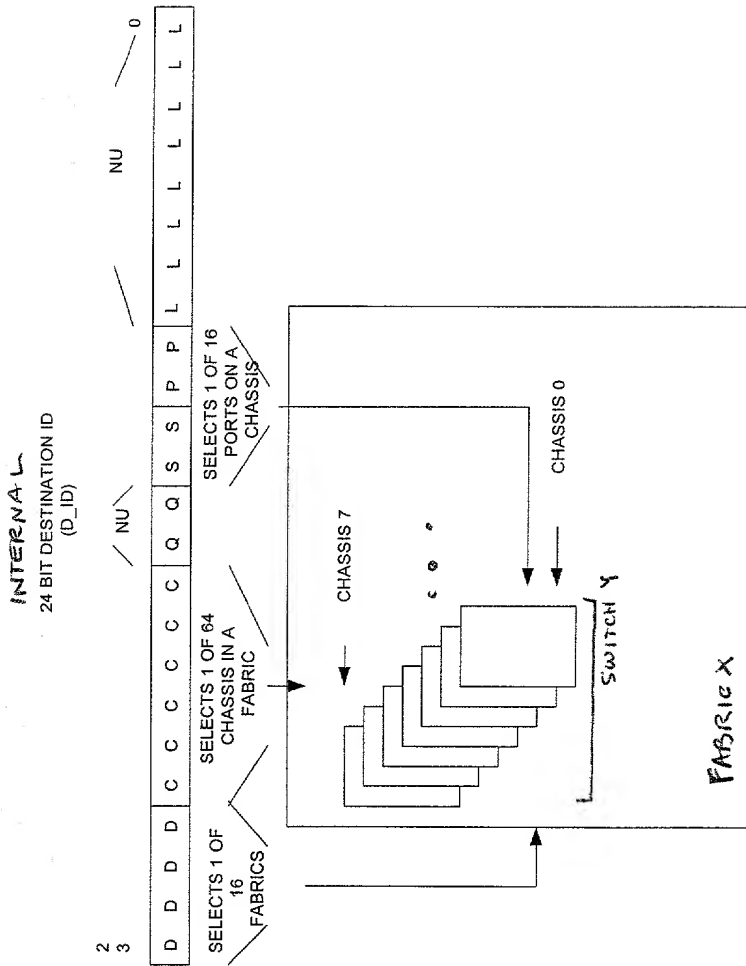


FIG. 13

500-0

Port Card 0, Switch #0, Chassis 0x00, Ports 1,3,5,7,9,B,D,F
Port Card 1, Switch #0, Chassis 0x01, Ports 1,3,5,7,9,B,D,F
Port Card 2, Switch #0, Chassis 0x02, Ports 1,3,5,7,9,B,D,F
Port Card 3, Switch #0, Chassis 0x03, Ports 1,3,5,7,9,B,D,F
Port Card 4, Switch #0, Chassis 0x04, Ports 1,3,5,7,9,B,D,F
Port Card 5, Switch #0, Chassis 0x05, Ports 1,3,5,7,9,B,D,F
Port Card 6, Switch #0, Chassis 0x06, Ports 1,3,5,7,9,B,D,F
Port Card 7, Switch #0, Chassis 0x07, Ports 1,3,5,7,9,B,D,F

502-0



500-7

Port Card 0, Switch #7, Chassis 0x38, Ports 1,3,5,7,9,B,D,F
Port Card 1, Switch #7, Chassis 0x39, Ports 1,3,5,7,9,B,D,F
Port Card 2, Switch #7, Chassis 0x3A, Ports 1,3,5,7,9,B,D,F
Port Card 3, Switch #7, Chassis 0x3B, Ports 1,3,5,7,9,B,D,F
Port Card 4, Switch #7, Chassis 0x3C, Ports 1,3,5,7,9,B,D,F
Port Card 5, Switch #7, Chassis 0x3D, Ports 1,3,5,7,9,B,D,F
Port Card 6, Switch #7, Chassis 0x3E, Ports 1,3,5,7,9,B,D,F
Port Card 7, Switch #7, Chassis 0x3F, Ports 1,3,5,7,9,B,D,F

502-7

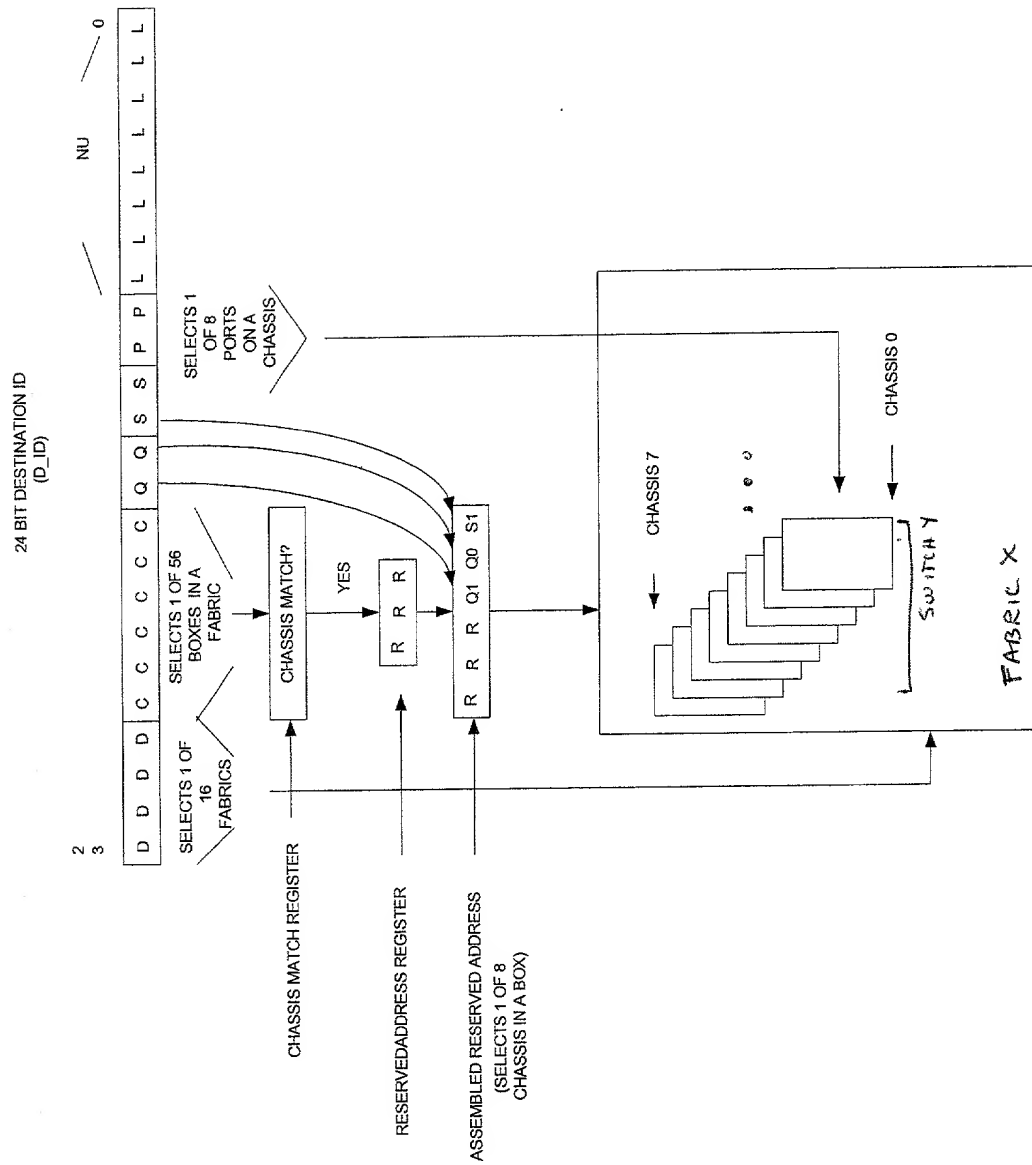


FIG. 15

600-0

Port Card 0, Switch #0, Chassis 0x00, Ports 0,1,2,3,4,5,6,7
Port Card 1, Switch #0, Chassis 0x00, Ports 8,9,A,B,C,D,E,F
Port Card 2, Switch #0, Chassis 0x00, Ports 10,11,12,13,14,15,16,17
Port Card 3, Switch #0, Chassis 0x00, Ports 18,19,1A,1B,1C,1D,1E,1F
Port Card 4, Switch #0, Chassis 0x00, Ports 20,21,22,23,24,25,26,27
Port Card 5, Switch #0, Chassis 0x00, Ports 28,29,2A,2B,2C,2D,2E,2F
Port Card 6, Switch #0, Chassis 0x00, Ports 30,31,32,33,34,35,36,37
Port Card 7, Switch #0, Chassis 0x00, Ports 38,39,3A,3B,3C,3D,3E,3F

602-0



600-55

Port Card 0, Switch #55, Chassis 0x37, Ports 0,1,2,3,4,5,6,7
Port Card 1, Switch #55, Chassis 0x37, Ports 8,9,A,B,C,D,E,F
Port Card 2, Switch #55, Chassis 0x37, Ports 10,11,12,13,14,15,16,17
Port Card 3, Switch #55, Chassis 0x37, Ports 18,19,1A,1B,1C,1D,1E,1F
Port Card 4, Switch #55, Chassis 0x37, Ports 20,21,22,23,24,25,26,27
Port Card 5, Switch #55, Chassis 0x37, Ports 28,29,2A,2B,2C,2D,2E,2F
Port Card 6, Switch #55, Chassis 0x37, Ports 30,31,32,33,34,35,36,37
Port Card 7, Switch #55, Chassis 0x37, Ports 38,39,3A,3B,3C,3D,3E,3F

602-55

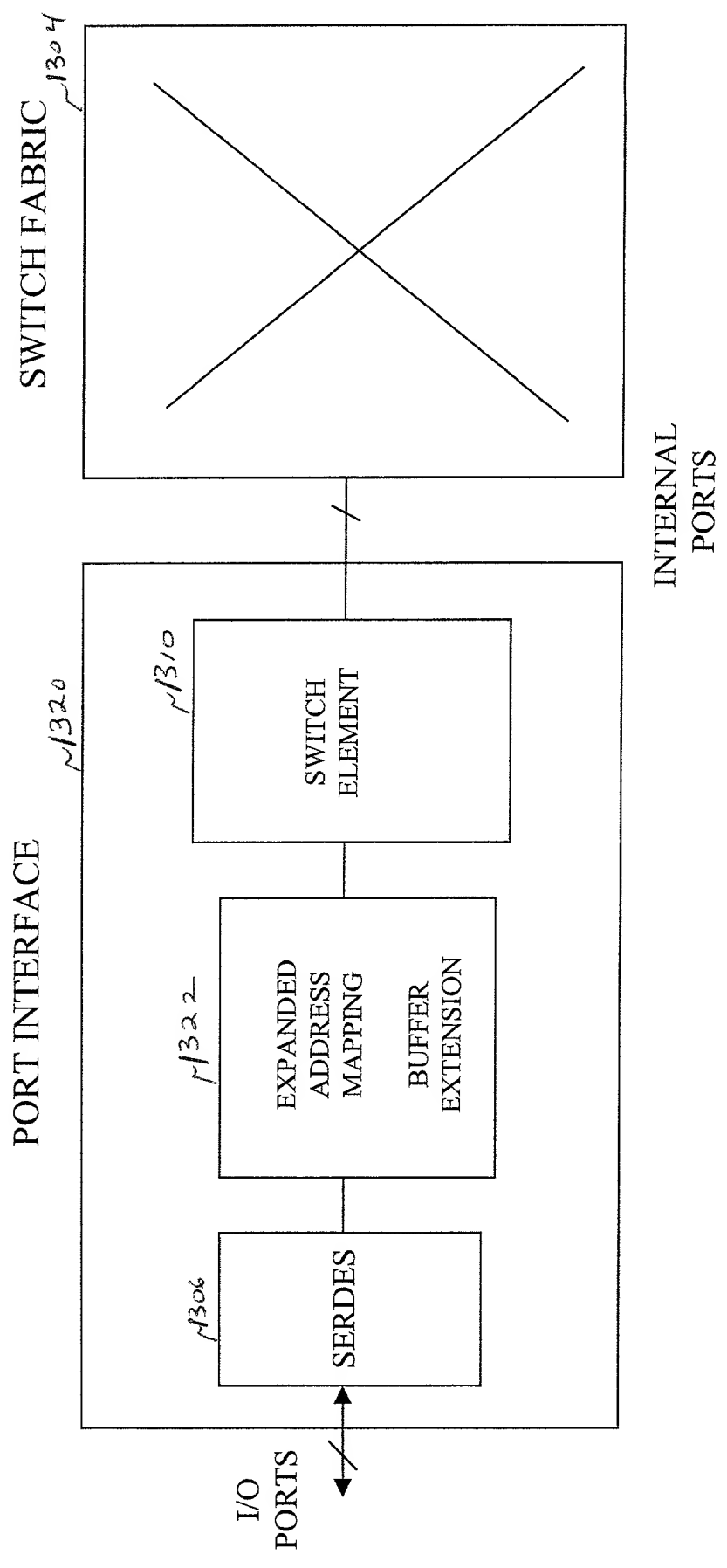


FIG. 17

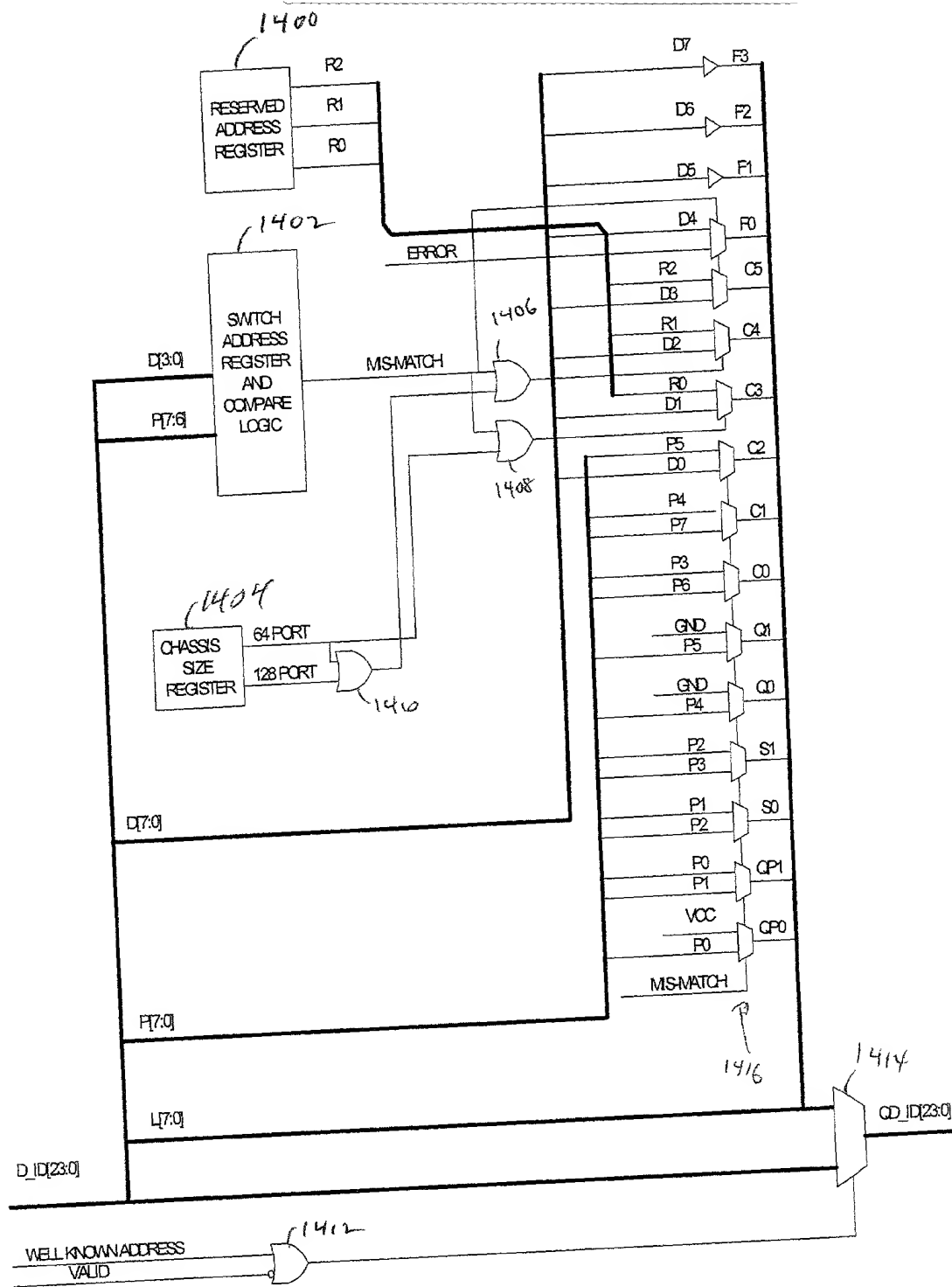
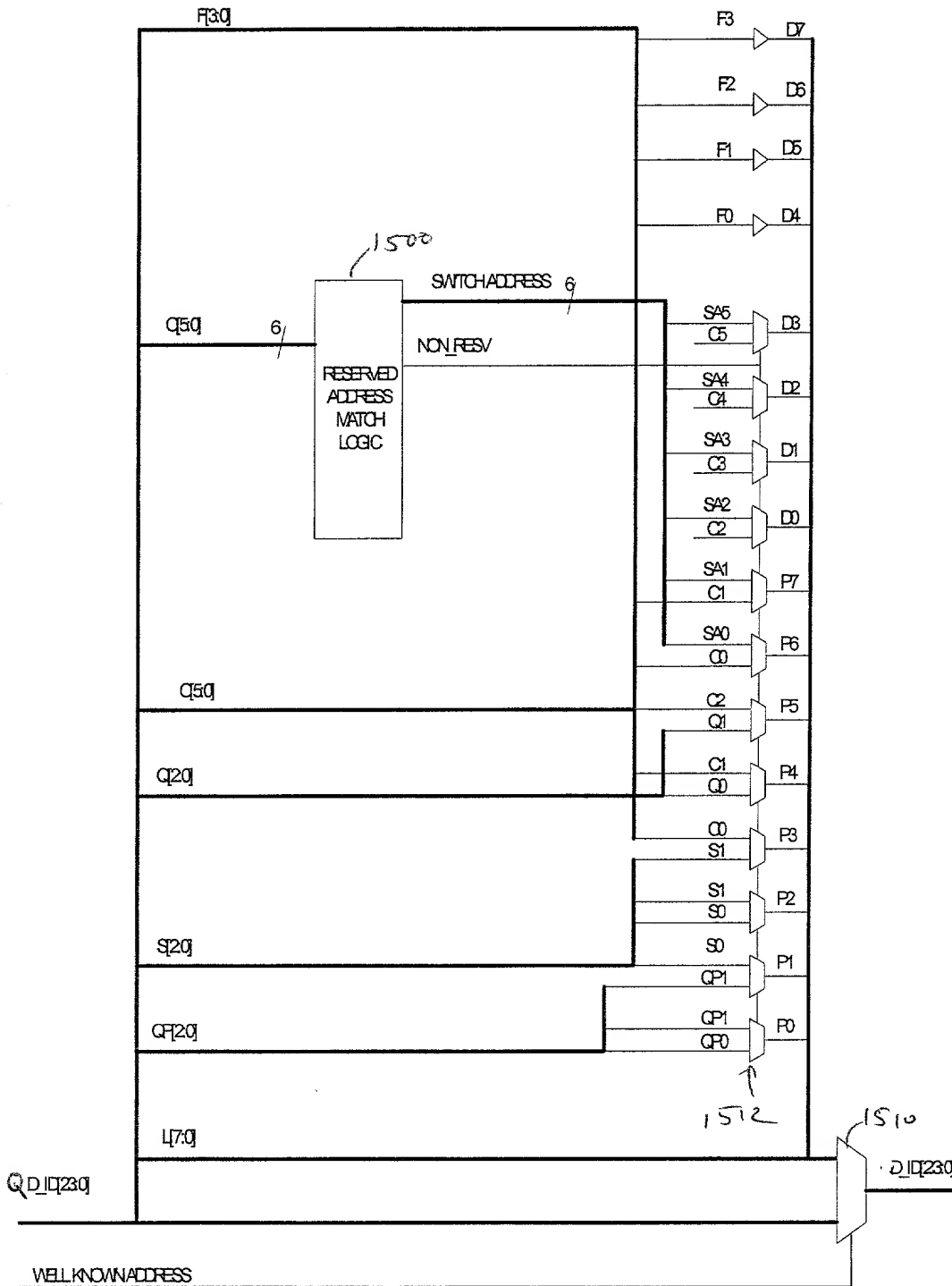


FIG. 18



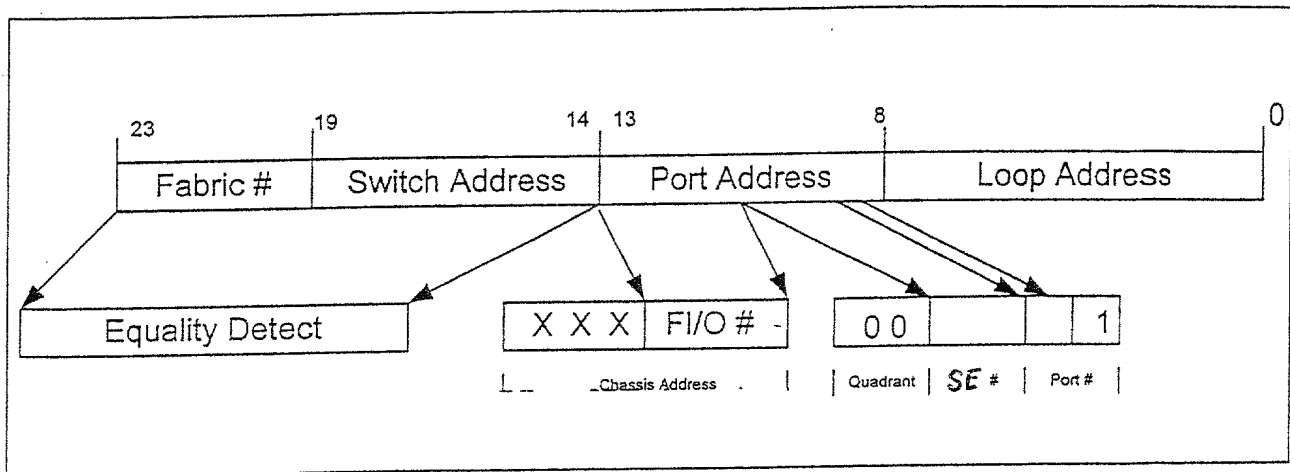


FIG. 20

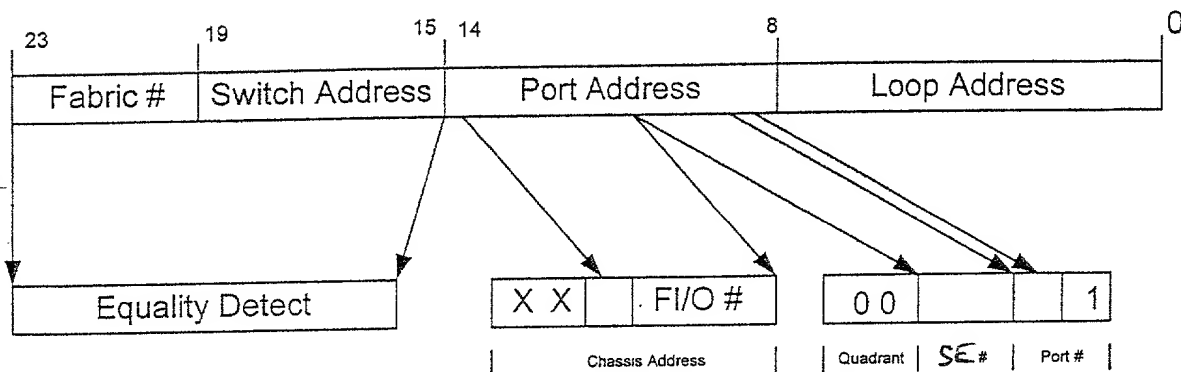


FIG. 21

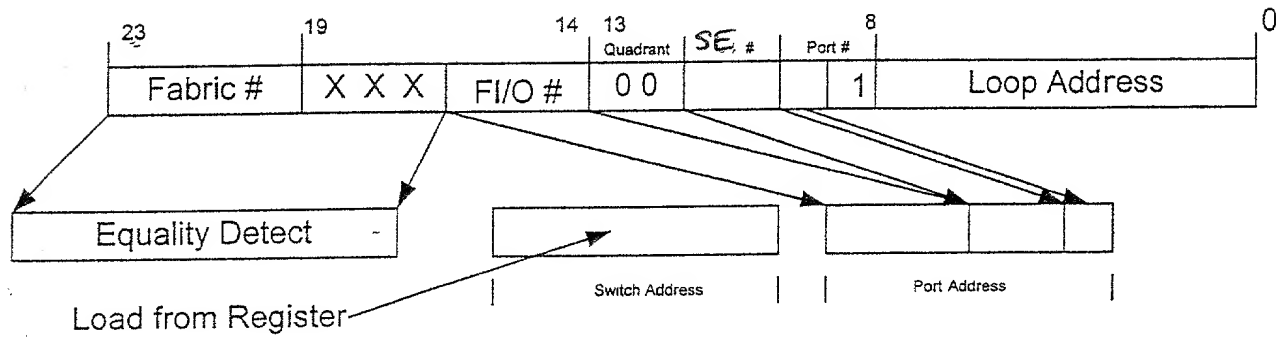


FIG. 22

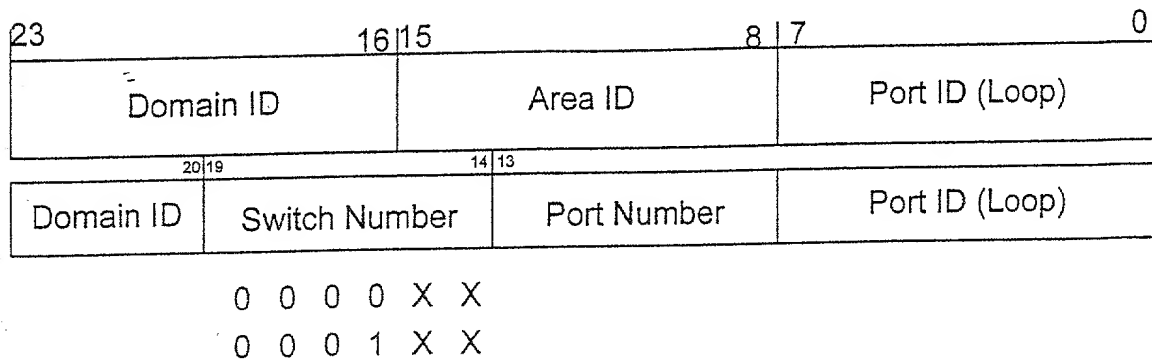


FIG. 23